UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/688,763 | 10/15/2003 | Sherman H. Yip | SUNMP360 | 1971 |

32291 7590 06/04/2007

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

| EXAMINER | |
|---|---|
| WANG, BEN C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2192 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/04/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/688,763 | YIP ET AL. | |
| | Examiner | Art Unit | |
| | Ben C. Wang | 2192 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *March 19, 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's amendment dated March 19, 2007, responding to the December 18, 2006 Office action provided in the rejection of claims 1-24, wherein claims 1-4, and 13-15 have been amended, claims 5-12, and 16-24 are remained as original.

Claims 1-24 remain pending in the application and which have been fully considered by the examiner.

Applicant's arguments with respect to claims rejection have been fully considered but are moot in view of the new grounds of rejection – see *Weaver et al.*, art made of record, as applied hereto.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory

action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Claim Rejections – 35 USC § 102(b)***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7-9, 11, 13-16, 19-21, and 23 and rejected under 35 U.S.C. 102(b) as being anticipated by Weaver et al. (*Performance Analysis Using Pipeline Visualization, 2001, IEEE)* (hereinafter 'Weaver')

3. **As to claim 1** (currently amended), Weaver discloses defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction (Sec. 2 – Related Work, visualizing a microprocessor is not a new idea. Past works have ranged from pedagogical pursuits to comprehensive performance studies; some of the existing visualization infrastructures to provide a context for the tool including "DLXview", "CPROF", "VTUNE", and "RIVET"; Fig. 2, elements of "coloring legend", "instruction window"); tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components by generating a graphical display

of a plurality of execution pipeline, each of which has indicia associated therewith that differs from the indicia associated with the remaining pipelines of said plurality of execution pipelines and placing a subset of said plurality of graphical icons adjacent to a first sub-portion of said indicia associated with one of said plurality of execution pipelines (Fig. 1 – overview the GPV usage flow; Fig. 2 - GPV Display Window, element of "instruction window"; Sec. 3 – Graphical Pipeline Views, this stream contains a detailed description of the instruction flow through the machine, documenting the movement of instructions in the pipeline from "birth" to "death"; in addition, the pipetrace stream denotes various other events and stage transitions that occur during an instruction's lifetime; multiple traces can be displayed on the screen at any given time for easy analysis); and displaying a progression of each of the plurality of graphical icons through the one or more hardware components during the execution of code segment by sequentially placing graphical icons of said subset adjacent to additional sub-portions of said indicia associated with said one of said plurality of execution pipelines (Fig. 2, element of "instruction window"; Sec. 3 – Graphical Pipeline Viewer – multiple traces can be displayed on the screen at any given time for easy analysis; Sec. 3.1 – main visualization window – this method for graphing instructions as they flow through a pipeline is a common visual representation, used in many textbooks including Hennessy and Patterson; the instruction axis contains tick mark to indicate the cycle count; additionally, the vertical axis will also display the instruction mnemonic when the window is zoomed in enough to fit legible text aside each instruction marks; the use of color (which can be

configured by the user) provides an effective means for spotting potential bottleneck; a highlight option which can flash the occurrences of a particular event, can be used as an alternative method of locating bottlenecks).

4. **As to claim 13** (currently amended), Weaver discloses program instructions for defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction (Sec. 2 – Related Work, visualizing a microprocessor is not a new idea. Past works have ranged from pedagogical pursuits to comprehensive performance studies; some of the existing visualization infrastructures to provide a context for the tool including "DLXview", "CPROF", "VTUNE", and "RIVET"; Fig. 2, elements of "coloring legend", "instruction window"); program instructions for tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components by generating a graphical display of a plurality of execution pipeline, each of which has indicia associated therewith that differs from the indicia associated with the remaining pipelines of said plurality of execution pipelines and placing a subset of said plurality of graphical icons adjacent to a first sub-portion of said indicia associated with one of said plurality of execution pipelines (Fig. 1 – overview the GPV usage flow; Fig. 2 - GPV Display Window, element of "instruction window"; Sec. 3 – Graphical Pipeline Views, this stream contains a detailed description of the instruction flow through the machine, documenting the movement of instructions in the pipeline

from "birth" to "death"; in addition, the pipetrace stream denotes various other events and stage transitions that occur during an instruction's lifetime; multiple traces can be displayed on the screen at any given time for easy analysis); and program instructions for displaying a progression of each of the plurality of graphical icons through the one ore more hardware components during the execution of the code segment by sequentially placing graphical icons of said subset adjacent to additional sub-portions of said indicia associated with said one of said plurality of execution pipelines (Fig. 2, element of "instruction window"; Sec. 3 – Graphical Pipeline Viewer – multiple traces can be displayed on the screen at any given time for easy analysis; Sec. 3.1 – main visualization window – this method for graphing instructions as they flow through a pipeline is a common visual representation, used in many textbooks including Hennessy and Patterson; the instruction axis contains tick mark to indicate the cycle count; additionally, the vertical axis will also display the instruction mnemonic when the window is zoomed in enough to fit legible text aside each instruction marks; the use of color (which can be configured by the user) provides an effective means for spotting potential bottleneck; a highlight option which can flash the occurrences of a particular event, can be used as an alternative method of locating bottlenecks).

5. **As to claim 2** (currently amended) (incorporating the rejection in claim 1), Weaver discloses that each of the icons of said subset having said displayable appearance with characteristic matching a characteristic of indicia associated

with said one of plurality of execution pipelines and distinguishable from characteristics of indicia associated with the remaining execution pipelines of said plurality of execution pipelines, when placed adjacent thereto (Fig. 2, element of "instruction window"; Sec. 3 – Graphical Pipeline Viewer – multiple traces can be displayed on the screen at any given time for easy analysis; Sec. 3.1 – main visualization window – this method for graphing instructions as they flow through a pipeline is a common visual representation, used in many textbooks including Hennessy and Patterson; the instruction axis contains tick mark to indicate the cycle count; additionally, the vertical axis will also display the instruction mnemonic when the window is zoomed in enough to fit legible text aside each instruction marks; the use of color (which can be configured by the user) provides an effective means for spotting potential bottleneck; a highlight option which can flash the occurrences of a particular event, can be used as an alternative method of locating bottlenecks).

6. **As to claims 3** (currently amended) (incorporating the rejection in claim 2), Weaver discloses the method and the computer readable medium wherein said sub-portion and said additional sub-portions define multiple sub-portions, each of which corresponds to clock cycle that differs from a clock cycle corresponding to the remaining sub-portions of said multiple sub-portions (Abstract, Lines 14-17; Sec. 3.1 – Main Visualization, 1st Para., Lines 4-10, 14-15 – the instruction window plots instructions in program order on a time axis space (measured in cycles), 5th Para., Lines 1-4, 6-9 – selecting an individual instruction

displays the cycle time of execution and the instruction mnemonic; the resource view allows resource graph lines to be selected, which returns the label, cycle number and instantaneous value; Sec. 3.2 – Pipetrace File Format, Line 2-4).

7. **As to claim 9** (original) (incorporating the rejection in claim 1), Weaver discloses that the method wherein the method operation of tracking each of the plurality of graphical icons includes, monitoring the plurality of graphical icons entering into the one or more hardware components; and monitoring the plurality of graphical icons departing from the one or more hardware components (Fig. 1 – overview the GPV usage flow; Fig. 2 - GPV Display Window, element of "instruction window"; Sec. 3 – Graphical Pipeline Views, this stream contains a detailed description of the instruction flow through the machine, documenting the movement of instructions in the pipeline from "birth" to "death").

8. **As to Claim 14** (currently amended) (incorporating the rejection in claim 13), Weaver discloses that the computer readable medium, wherein said program instruction for defining further includes a sub-routine to provide each of the icons of said subset with said displayable appearance having characteristics matching a characteristic of indicia associated with said one of plurality of execution pipelines and distinguishable form characteristics of indicia associated with the remaining execution pipelines of said plurality of execution pipelines, when placed adjacent thereto (Fig. 2, element of "instruction window"; Sec. 3 – Graphical Pipeline Viewer – multiple traces can be displayed on the screen at

any given time for easy analysis; Sec. 3.1 – main visualization window – this method for graphing instructions as they flow through a pipeline is a common visual representation, used in many textbooks including Hennessy and Patterson; the instruction axis contains tick mark to indicate the cycle count; additionally, the vertical axis will also display the instruction mnemonic when the window is zoomed in enough to fit legible text aside each instruction marks; the use of color (which can be configured by the user) provides an effective means for spotting potential bottleneck; a highlight option which can flash the occurrences of a particular event, can be used as an alternative method of locating bottlenecks).

9. **As to Claim 15** (currently amended) (incorporating the rejection in claim 14), Weaver discloses the computer readable medium wherein said sub-portion and said additional sub-portions define multiple sub-portions and further including a sub-routine to correspond each of said multiple sub-portions with a clock cycle that differs from a clock cycle corresponding to the remaining sub-portions of said multiple sub-portions (Abstract, Lines 14-17; Sec. 3.1 – Main Visualization, 1st Para., Lines 4-10, 14-15 – the instruction window plots instructions in program order on a time axis space (measured in cycles), 5th Para., Lines 1-4, 6-9 – selecting an individual instruction displays the cycle time of execution and the instruction mnemonic; the resource view allows resource graph lines to be selected, which returns the label, cycle number and instantaneous value; Sec. 3.2 – Pipetrace File Format, Line 2-4).

10. **As to claim 4** (currently amended) (incorporating the rejection in claim 1) and **Claim 16** (original) (incorporating the rejection in claim 13), Weaver discloses displaying the progression of each of the plurality of instructions includes, displaying a tabular view of the progression of each of the plurality of instructions through the one or more hardware components during the execution of the code segment (Fig. 3 – sample pipetrace stream; Sec. 3.2 – Pipetrace File Format).

11. **As to claim 7** (original) (incorporating the rejection in claim 1) and **19** (original) (incorporating the rejection in claim 13), Weaver discloses that the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color (Fig. 2 – GPV Display Window, element of "Instruction Window"; Fig. 5).

12. **As to claim 8** (original) (incorporating the rejection in claim 1) and **Claim 20** (original) (incorporating the rejection in claim 13), Weaver discloses that the progression is movement between the one or more hardware components through intervals of time (Sec. 3.1 – Main Visualization Windows, 1st Para., Lines 4-5 – the instruction window plots instructions in program order on a time axis space, 2nd Para., Lines 10-11 – both the resource and instruction views are plotted against simulator time on the x-axis).

13. **As to claim 11** (original) (incorporating the rejection in claim 1) and **Claim 23** (original) (incorporating the rejection in claim 13), Weaver discloses that the

execution of the code segment generates the instructions to the one or more hardware components (Sec. 1 – Introduction, 3rd Para., Lines 7-9; Sec. 4.3 – Hardware performance analysis).

14. **As to claim 21** (original) (incorporating the rejection in claim 13), Weaver discloses that the computer readable medium wherein the program instructions for tracking each of the plurality of graphical icons includes, program instructions for monitoring the plurality of graphical icons entering into the one or more hardware components; and program instructions for monitoring the plurality of graphical icons departing from the one or more hardware components (Fig. 1 – overview the GPV usage flow; Fig. 2 - GPV Display Window, element of "instruction window"; Sec. 3 – Graphical Pipeline Views, this stream contains a detailed description of the instruction flow through the machine, documenting the movement of instructions in the pipeline from "birth" to "death").

***Claim Rejections – 35 USC § 103(a)***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weaver in view of Wong et al. (*US Patent No. 6,175,364 B1*) (hereinafter 'Wong')

16. **As to claim 5** (original) (incorporating the rejection in claim 1) and **claim 17** (original) (incorporating the rejection in claim 13), Weaver does not disclose selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons.

However, in an analogous art, Wong discloses selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons (Col. 1, lines 22-31).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Weaver with the teachings of Wong to further provide selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons in Weaver system.

The motivation is to provide end-users for visualizing relatively large amounts of data in a limited display space as once suggested by Wong (Col. 2, lines 34-37).

17. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weaver in view of Wong and further in view of Drongowski et

al. (*Profiling to Tune C Programs on Alpha, April 6, 2001, Hewlett Packard Company*) (hereinafter 'Drongowski')

18. **As to claim 6** (original) (incorporating the rejection in claim 5) and **18** (original) (incorporating the rejection in claim 17), Weaver and Wong do not specifically disclose that the information is defined by one or more of a name of the instruction, an internal representation of the instruction, a program counter associated with an instruction, a physical memory location of the instruction, an instruction disassembly, a register source, a register destination, a virtual addresses of data, and a physical address of the data to be loaded.

However, in an analogous art, Drongowski discloses that the information is defined by one or more of a name of the instruction (P. 23, Alpha no-op Instructions, Mnemonic), an internal representation of the instruction (P. 26, bottom area, 0x120001190), a program counter associated with an instruction (P. 26, bottom area, :count), a physical memory location of the instruction (P. 32, 0x120001150 for example), an instruction disassembly (P. 23, Alpha no-op Instructions, Disassembly), a register source (P. 23, Alpha no-op Instructions, Mnemonic, Rx for example), a register destination (P. 23, Alpha no-op Instructions, Mnemonic, R31 for example), a virtual addresses of data (P. 33, Sec. 5.4.3), and a physical address of the data (P. 33, Sec. 5.4.3) to be loaded.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Weaver and Wong

with the teachings of Drongowski to further provide performance tuning mechanism in Weaver-Wong system.

The motivation is to provide performance tuning to identify and remove bottleneck as once suggested by Drongowski (i.e. Sec. 1.0).

19. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weaver in view of Hollingsworth et al. (*The Clipper Processor: Instruction Set Architecture And Implementation, February 1989, ACM*) (hereinafter 'Hollingsworth') and further in view of Sherwood et al. (*A Pipelined Memory Architecture for High Throughput Network Processors, June 2003, IEEE*) (hereinafter 'Sherwood')

20. **As to claim 10** (original) (incorporating the rejection in claim 1) and **22** (original) (incorporating the rejection in claim 13), Weaver does not disclose that the one or more hardware components is defined by one or more of an instruction buffer, an integer instruction execution pipeline, a loads and stores execution pipeline, a branch execution pipeline, a floating point add execution pipeline, a floating point multiply execution pipeline, a microprocessor, an address switch, a data switch, a memory controller, an Ethernet, a network, a data cache, a memory, a bus, an interconnect, a motherboard routing, and a protocol.

However, in an analogous art, Hollingsworth discloses that the one or more hardware components is defined by one or more of an instruction buffer (Sec. of Bit Ordering, 2nd paragraph, lines 5-10; Sec. of Instruction Bus Interface,

1st paragraph, lines 1-5; Fig. 4, entity of Instruction Bus Interface, Instruction Buffer), an integer instruction execution pipeline (Fig. 4, entity of Integer Execution Unit; Fig. 6, entity of Integer Execution Unit), a loads and stores execution pipeline (Sec. of Motivation and Design Philosophy, 4th paragraph, lines 7-13; Sec. of INSTRUCTION FORMATS AND ADDRESSING MODES, Addressing Modes, 1-11), a branch execution pipeline (Sec. of Branches and Condition Codes; Table III, Branch Logic), a floating point add execution pipeline (Fig. 4, entity of Floating Point Execution Unit; Fig. 5, entity of Floating Point Unit; Fig. 6, entity of Floating Point Execution Unit), a floating point multiply execution pipeline (Fig. 4, entity of Floating Point Execution Unit; Fig. 5, entity of Floating Point Unit; Fig. 6, entity of Floating Point Execution Unit), a microprocessor (Fig. 1, entity of CPU/FPU), an address switch (1st Sec., 1st paragraph, lines 10-20), a data switch (1st Sec., 2nd paragraph, lines 1-11; Sec. of Address Space), a memory controller (Sec. of Memory Architecture and Data Types, Memory Architecture), a data cache (1st Sec., 1st paragraph, lines 1-5; Sec. of Caching), a memory (Fig. 1, entity of MAIN MEMORY), a bus (Fig. 5, entity of Instruction Bus Interface, Instruction Bus to I-CAMMU, entity of Data Bus Interface, Data Bus to D-CAMAU; Fig. 1, entity of CLIPPER BUS; Sec. of Data Bus Interface), an interconnect (Fig. 5, bold arrow lines; Table III, Other - Interconnect), and a protocol (Sec. of Tradeoffs And Extensions, Better Multiprocessor Cache Consistency, lines 1-5).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Weaver and the

teachings of Hollingsworth to further provide those hardware components in Weaver system.

The motivation is to provide high performance, cost effectiveness, convenient programmability, and an architecture that can be expanded as technology improvise and the an of computer architecture design advances as once suggested by Hollingsworth (i. e., Sec. of Conclusions).

Furthermore, Weaver and Hollingsworth do not disclose an Ethernet, a network, a motherboard routing.

However, in an analogous art, Sherwood discloses a network (Fig. 1; Sec. 3), a motherboard routing (Fig. 2; Fig. 3; Sec. 2.1; Sec. 2.2). Official Notice is taken that an Ethernet is well known in the art.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Weaver and Hollingsworth with the teachings of Sherwood to further provide routing and networking components in Weaver-Hollingsworth system.

The motivation is to provide a programmable and scalable network processor solution for next generation backbone routers as once suggested by Sherwood (i.e. Sec. of Summary).

21. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weaver in view of Hollingsworth.

22. **As to claim 12** (original) (incorporating the rejection in claim 1) and **24** (original) (incorporating the rejection in claim 13), Weaver does not disclose that the plurality of instructions of the code segment are defined by one or more of a load instruction, an add instruction, a subtract instruction, a store instruction, a branch instruction, a register movement instruction, a shift instruction, an input instruction, and an output instruction.

However, in an analogous art, Hollingsworth discloses that the plurality of instructions (Table II. Operations and Opcodes, Instruction Type, Variants and Op Codes) of the code segment are defined by one or more of a load instruction (LOAD), an add instruction (ADD), a subtract instruction (SUBTRACT), a store instruction (STORE), a branch instruction (BRANCH CONDITIOANL; BRANCH FLOATING EXCEPTION), a register movement instruction (SAVE REGISTERS; RESTORE REGISTERS), a shift instruction (SHIFT ARITHMETIC; SHIFT LOGICAL), an input instruction (LOAD address(loada); LOAD byte(loadb)), and an output instruction STORE word(storw); STORE byte(storb)).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Weaver and the teachings of Hollingsworth to further provide those instructions in Weaver system.

The motivation is to provide an instruction set for convenient and efficient programmability, and it can be easily implemented in hardware as once suggested by Hollingsworth (i.e., Sec. of Instruction Set).

***Conclusion***

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Campenhout et al., ESCAPE: Environment for the Simulation of Computer Architectures for the Purpose of Education, 1998, University of Ghent
- Gomez et al., Method and Apparatus for Visualization of Microprocessor Pipeline Operation (Pub. No. US 2002/0062208 A1)

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BCW

TUAN DAM
SUPERVISORY PATENT EXAMINER

May 18, 2007